

**JUNE 23-27, 2024**

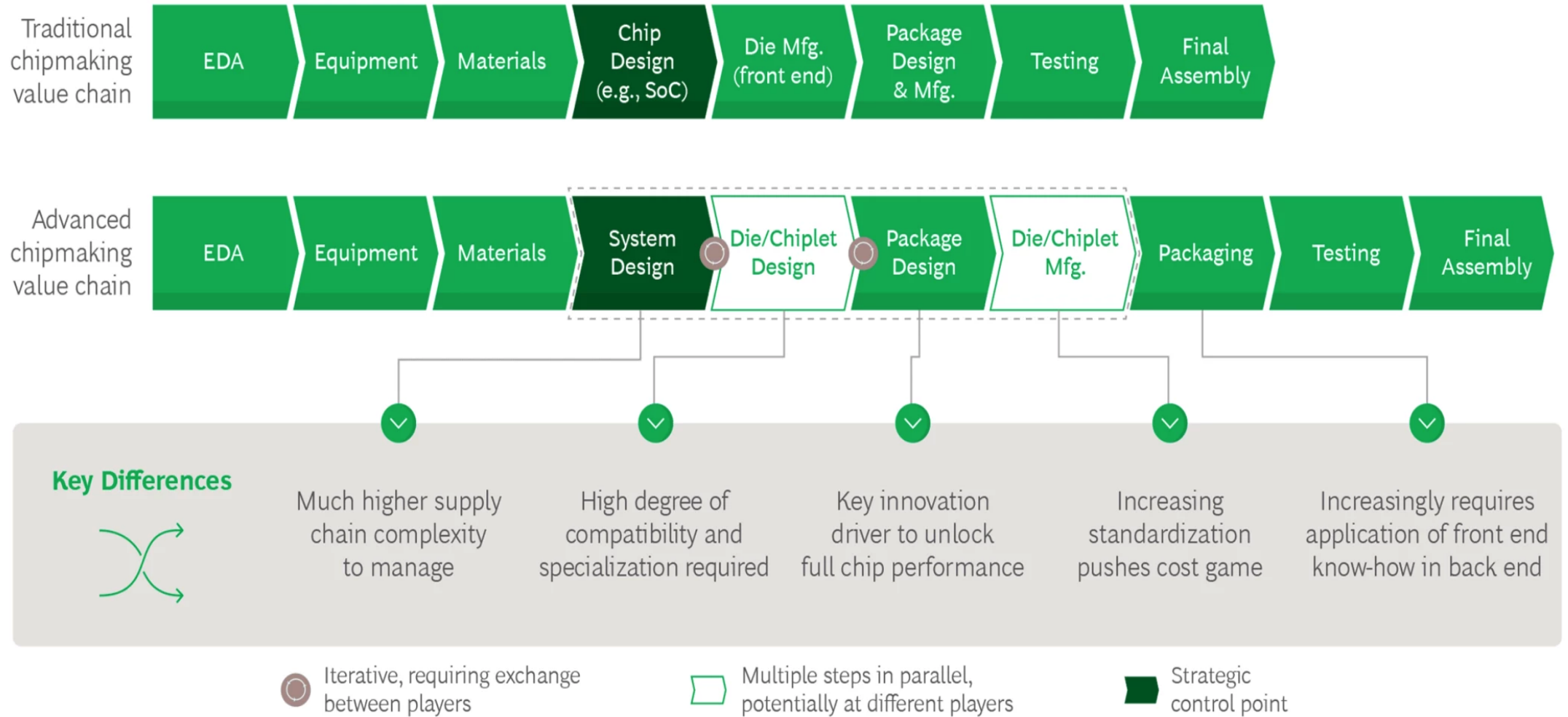
MOSCONE WEST CENTER  
SAN FRANCISCO, CA, USA

# Adv Packaging for AI Era

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Co-founder & CEO

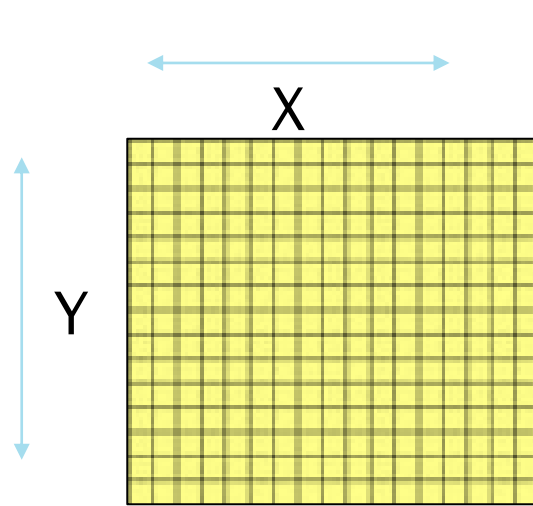


# Advanced Packaging New Value Chain

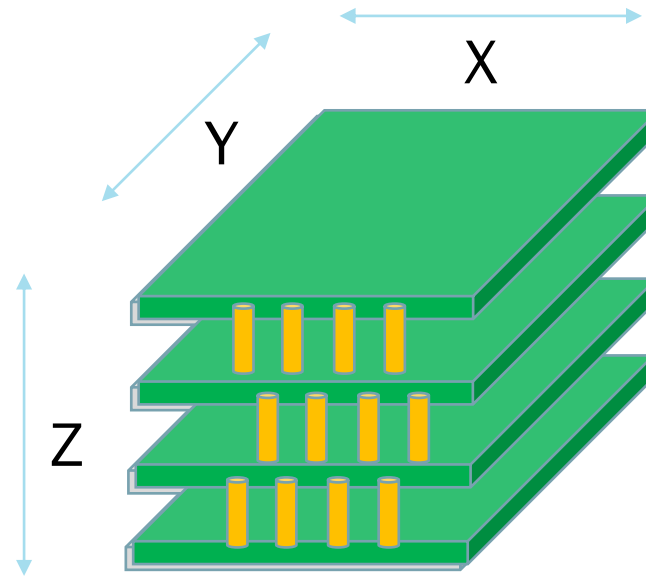
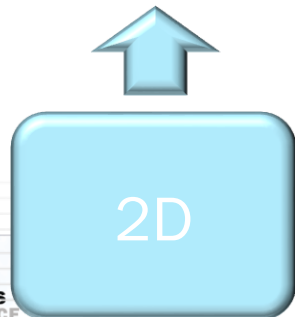


Source: BCG

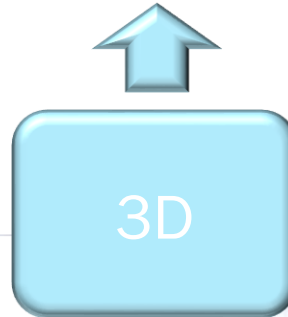
# Evolution of Integration Platforms:



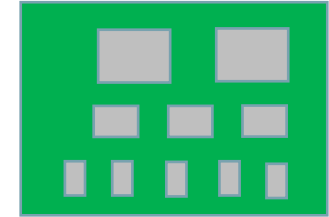
Moore's Law



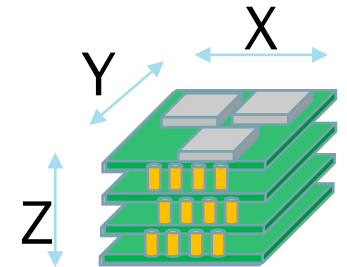
3D Packaging  
(Monolithic Chips)



Advanced Packaging



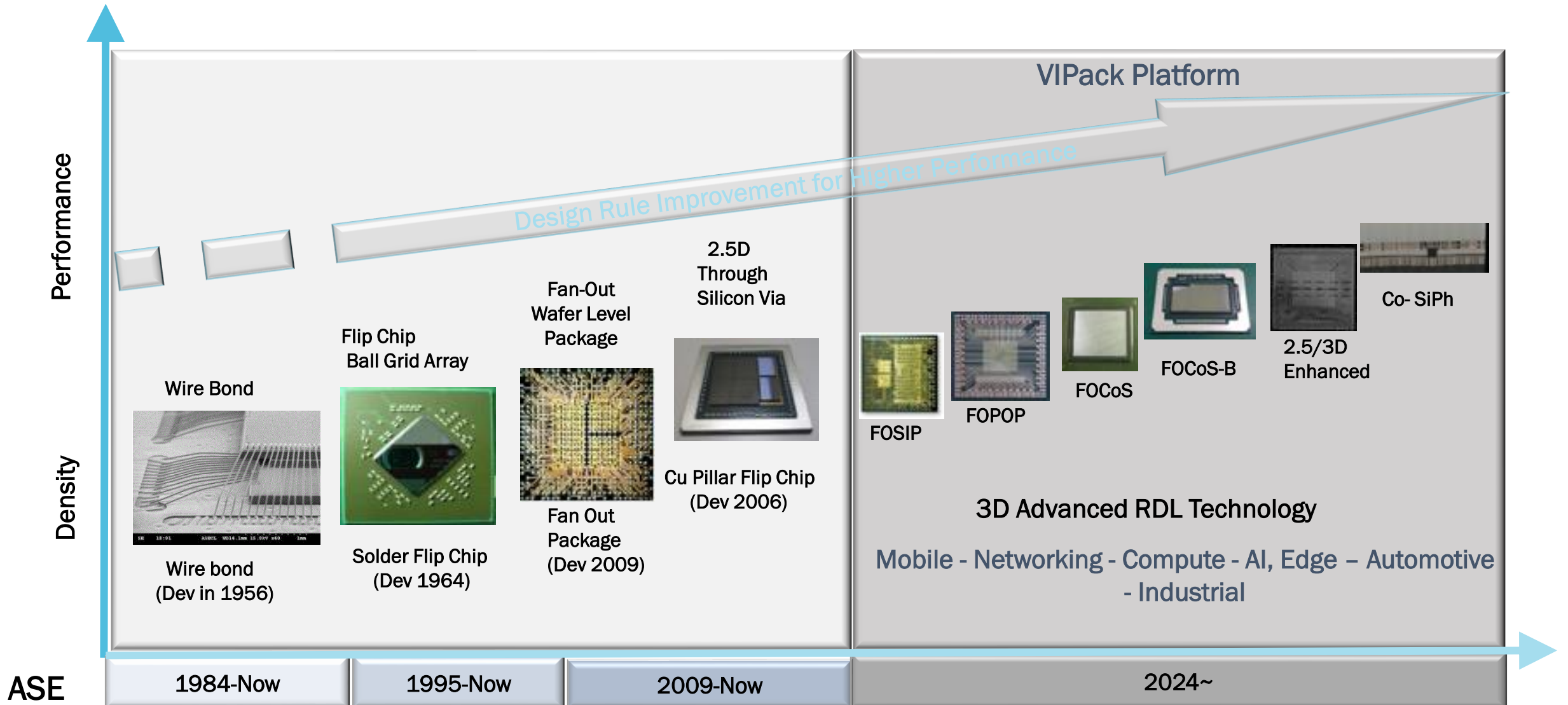
Shrink Heterogeneous Systems (HD RDL)



Stacking Heterogeneous  
Systems (Open Ecosystem)

Domain Specific  
Architecture & System  
Integration

# Advanced Packaging Roadmap



# FOPoP

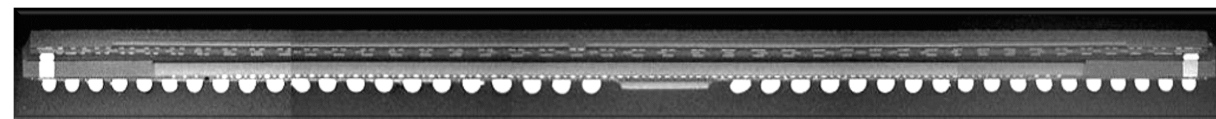
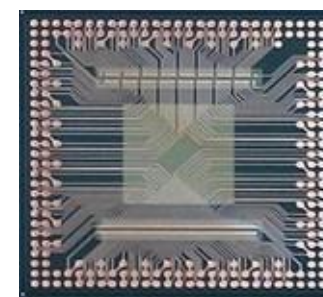
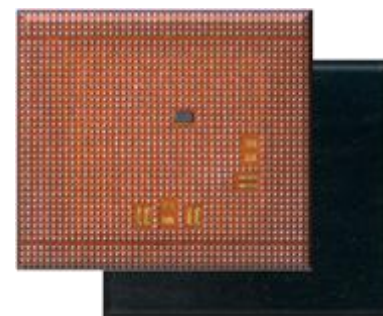
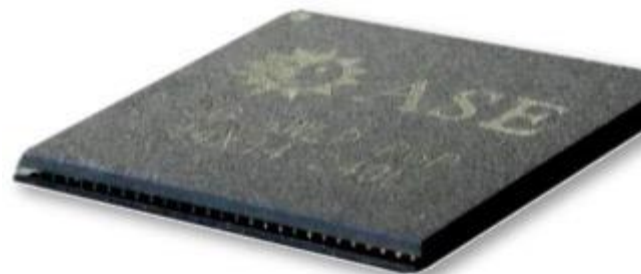


## Key Features:

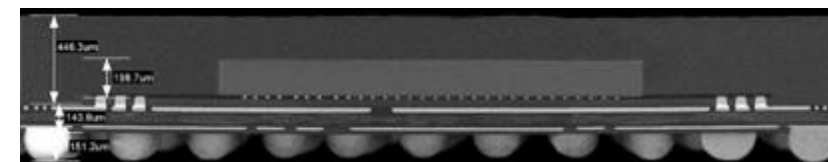
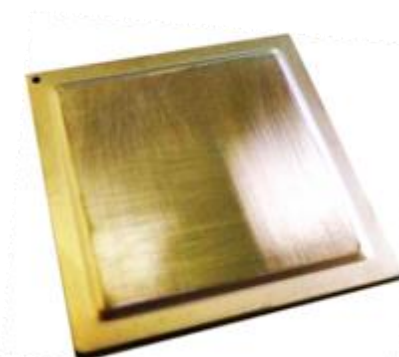
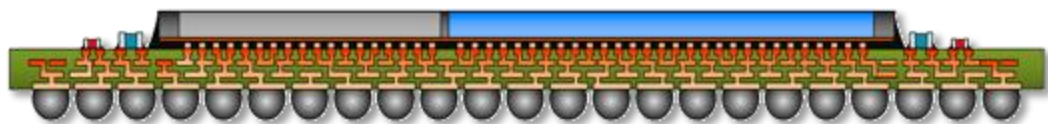
- FOPoP: Fan Out Package-on-Package
- RDL Based Package with 2 Routing Planes and Fine Pitch Cu Posts Between Layers
- Bottom Package Height <330um
- Land Side Cap or Embedded DTC (M)
- Cu Post Pitch ~140um (@100um Die)
- Power Delivery Solution with Near
- Die DTC (Adv. Silicon Node)

## Applications:

- Application Processor (AP) Mobile
- Co-Package SiPh
- Mobile/Auto AIP (Antenna-In-Package)

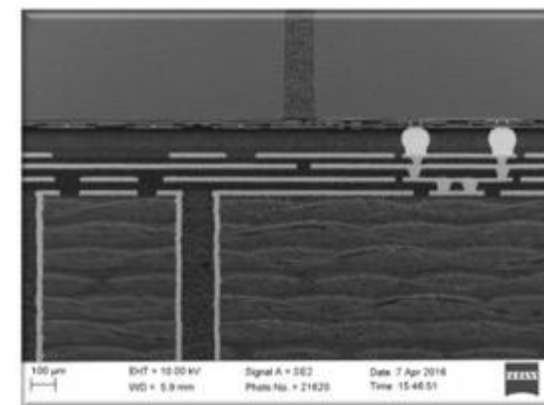


# FOCoS



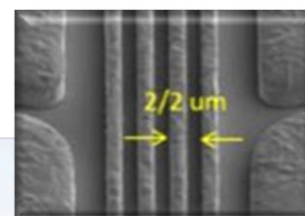
## Key Features:

- High Density Fan-Out Single or Multi Die Integration Package-Chip First or Chip Last
- 1.5/1.5um Line/Space, 6 metal layers, 32x38mm FO
- Flip Chip attached to RDL or Organic Substrate
- Stacked Via for Low Impedance
- Support HBM2/3 Integration

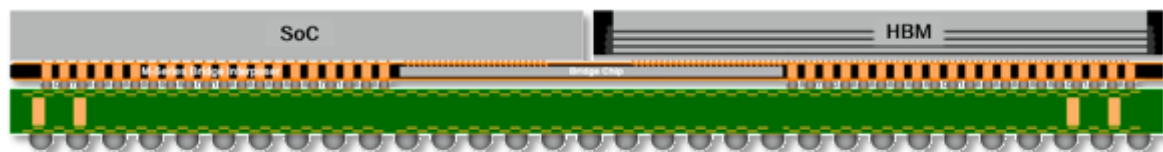


## Applications:

- APU + Memory
- GPU + Memory
- Networking
- SiP/Modules
- AI



# FOCoS Bridge (Embedded)

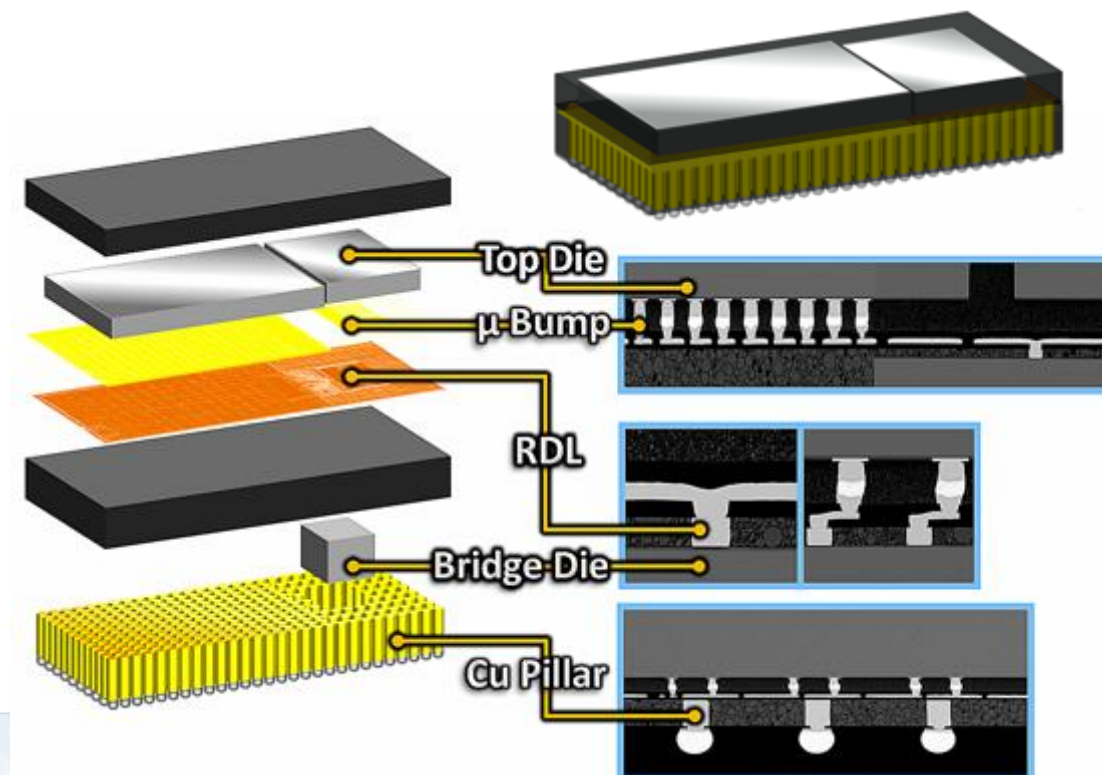
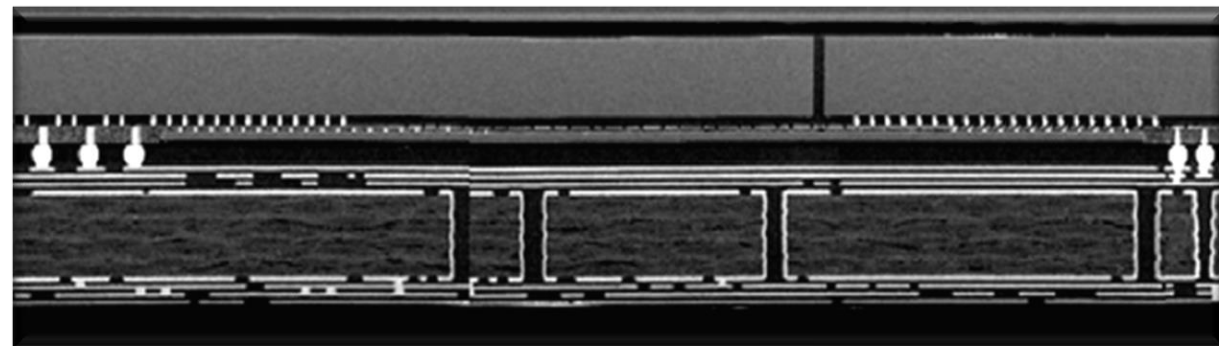


## Key Features:

- Embedded Die Layer- Die Attached on Both Sides of RDL (Bridge, DTC, Power Mgmt, Active)
- High Density Fan-Out Single or Multi Die Integration Package- Chip First or Chip Last
- 1.5/1.5um Line/Space, 6 metal layers, 32x38mm FO
- Flip Chip attached to RDL or Organic Substrate
- Lower Cross Talk (No TSV)

## Applications:

- APU + Memory
- GPU + Memory
- Switching/Router-Networking/AI
- SiP/Modules



# FOSiP

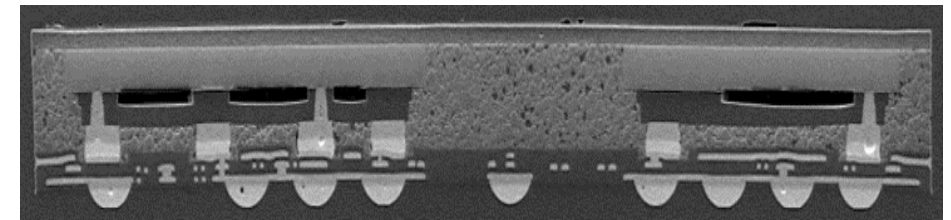
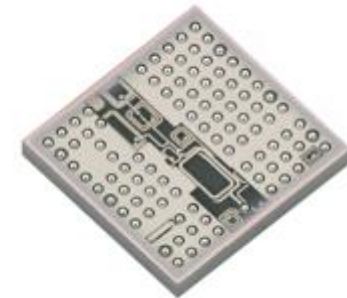
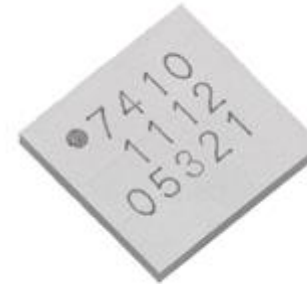
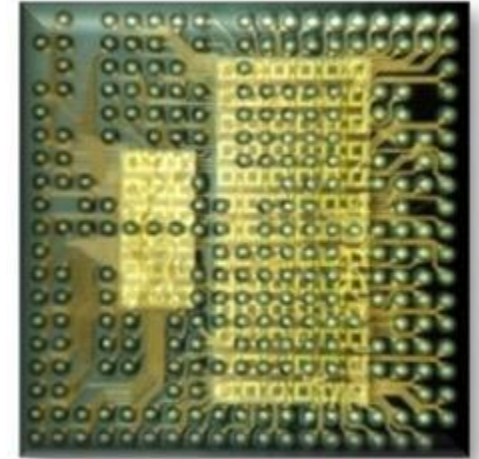


## Key Features:

- FOSiP: Fan-Out System in Package
- Lowest Profile Structure
- Ultra High-Density Component spacing- 50um
- Multi Layer RDL Substrate Layer
- Integration of both un-packaged and packaged components
- The option for double sided
- RDL – Chip Last for Std Component Termination

## Applications:

- Mobile - RFFEM
- IoT- WIFI
- Auto - Radar



# 2.5D/3D TSV

## Key Features:

### 2.5D Chiplet Integration:

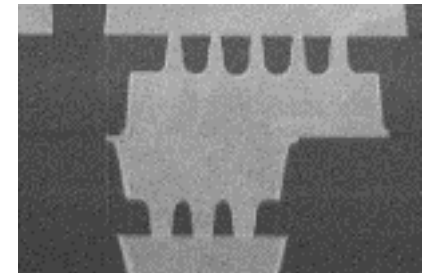
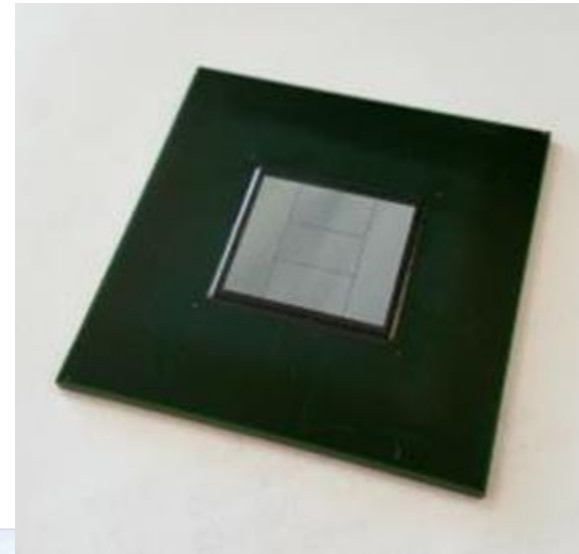
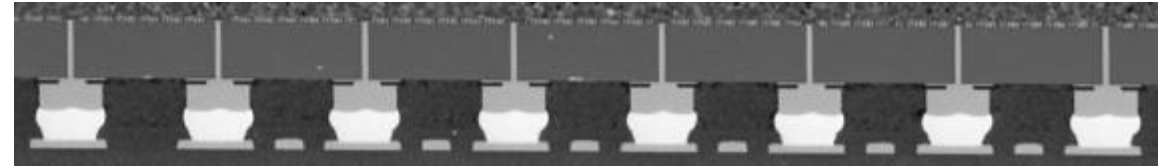
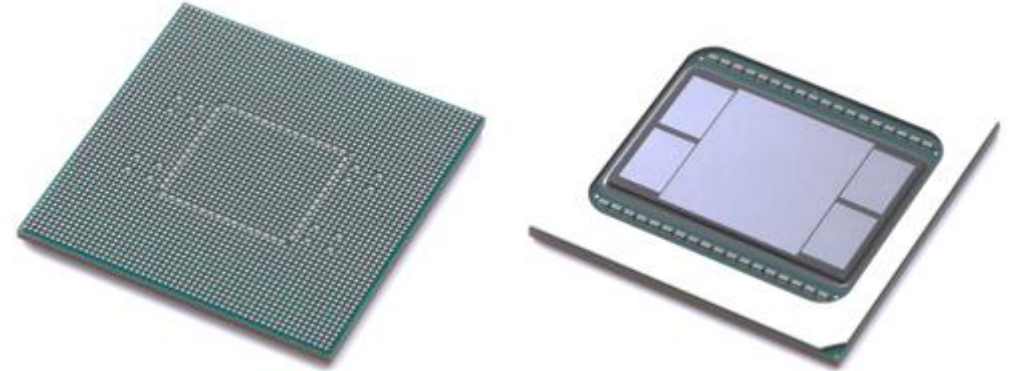
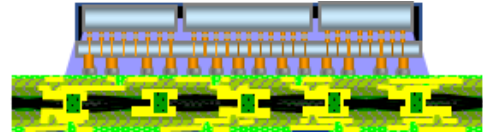
- Stitched interposer > 1.6x reticle
- Interposer BEOL RDL Passive Integration Options
- Fine Pitch D2D Interconnects:  $\mu\text{Bump pitch} \leq 45\mu\text{m}$ ,  $L/S \leq 1\mu\text{m}$ , up to 5 layers

### 3.5 D Die Stacking + Hybrid Bonding Innovations:

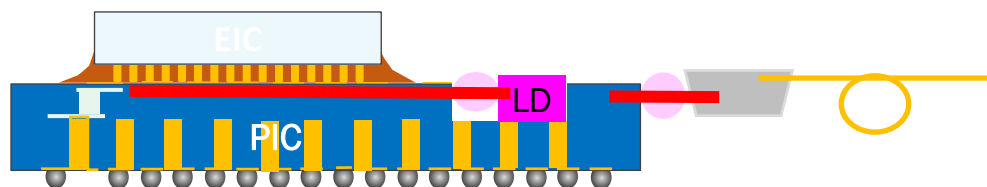
- Active interposer: DRAM Interposer - high memory bandwidth & energy efficiency
- 3D die stacking: DRAM die stacking - high memory bandwidth & capacity
- Ultra Fine Pitch Interconnects: Bond pitch <  $30\mu\text{m}$

## Applications:

- High Power Computing, Networking, Mobile



# Integrated Optics

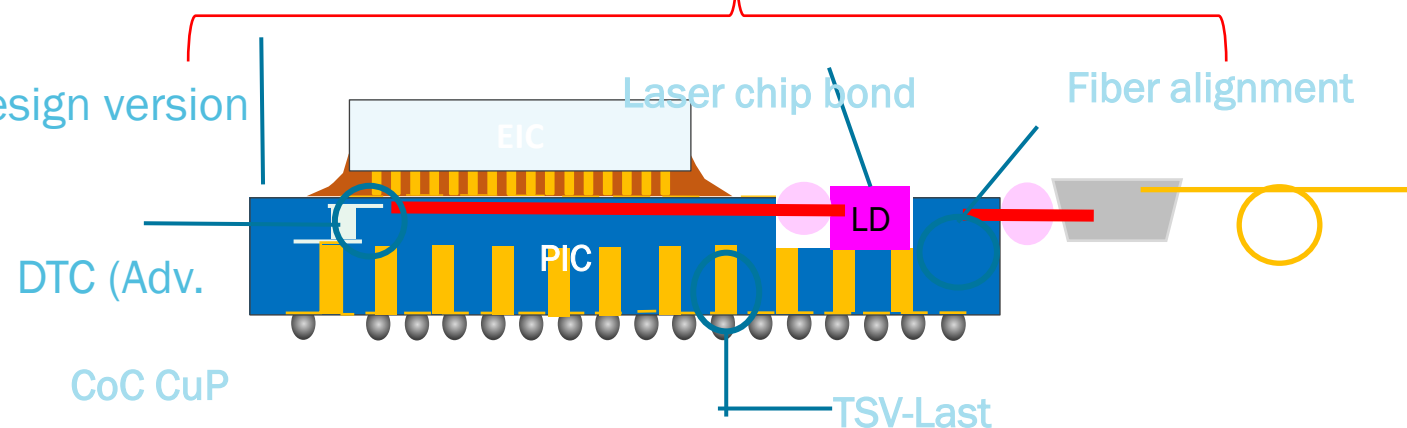
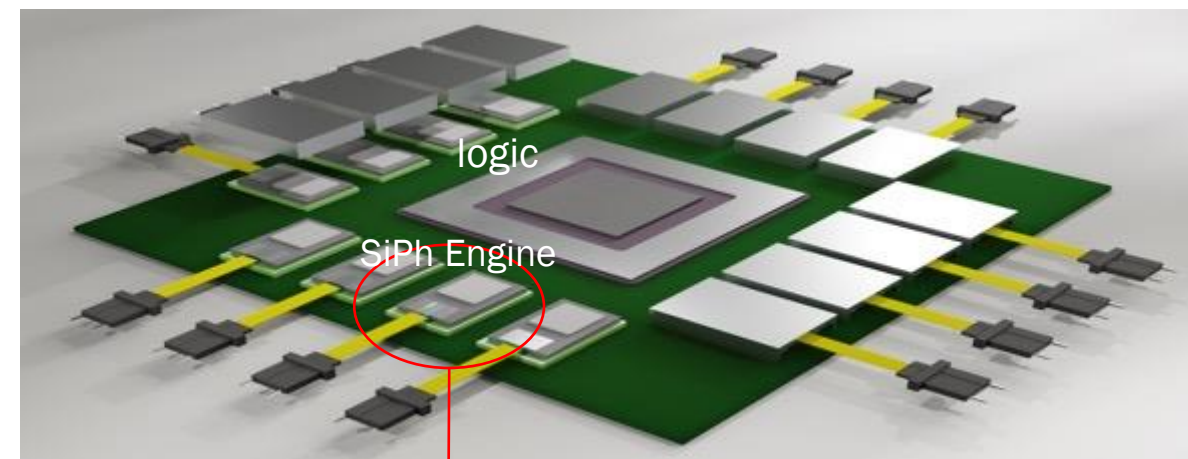


## Key Features:

- Replaces Traditional SERDES HS Interface
- RDL Based Package with 2 Routing Planes and Fine Pitch Cu Posts Between Layers
- MicroBump- 45um pitch, 30um Diam
- 2 RDL Layers
- TSV Last Pitch 60um dia, 140um pitch- Slot design version
- 30um dia, 60um pitch
- V-Groove for Alignment- DRIE Process
- Power Delivery Solution with Near Die Silicon Node)

## Applications:

- ASIC on Network Switch
- Stand Alone Laser Engine- For High Speed



# Summary

- AI and Data continue to fuel semiconductor innovation, with exponential proliferation through 2030 and beyond that will shape global life and lifestyle in unimaginable ways
- Collectively, our industry is accelerating the AI economy through Heterogeneous Integration advancements
- Packaging creativity is enabling seamless integration of multiple chiplets, SiPs, modules into one single package optimized for enhanced functionality and operating characteristics.

